

FIG 2

FIG.3

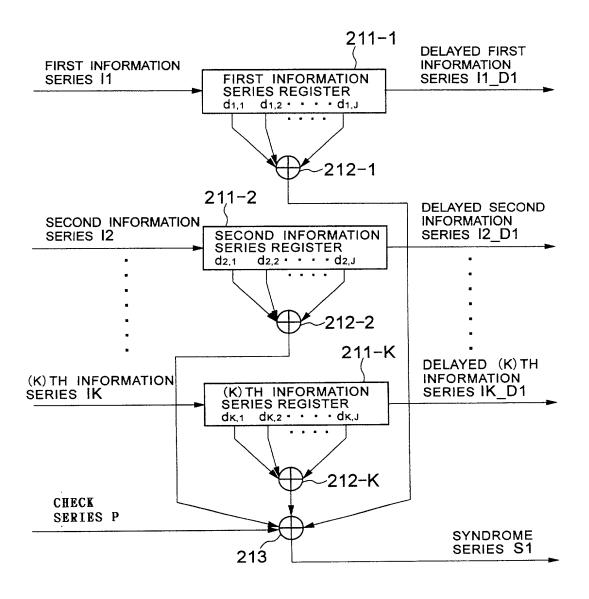


FIG.4

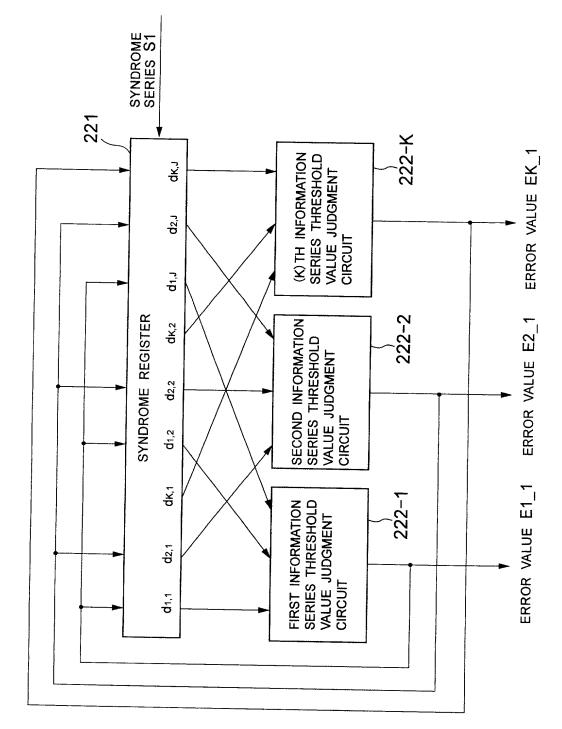


FIG. 5

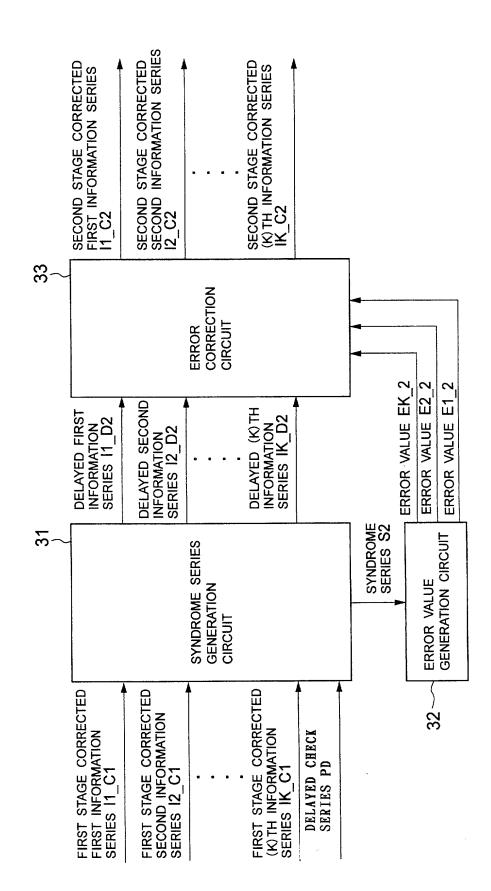


FIG.6

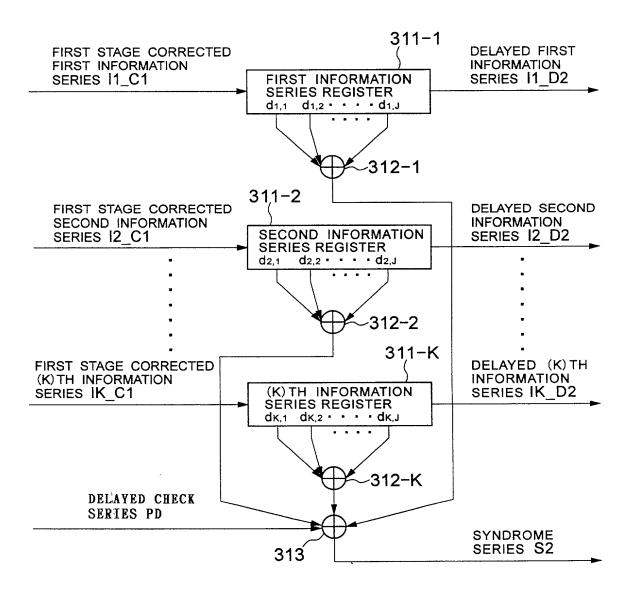


FIG.7

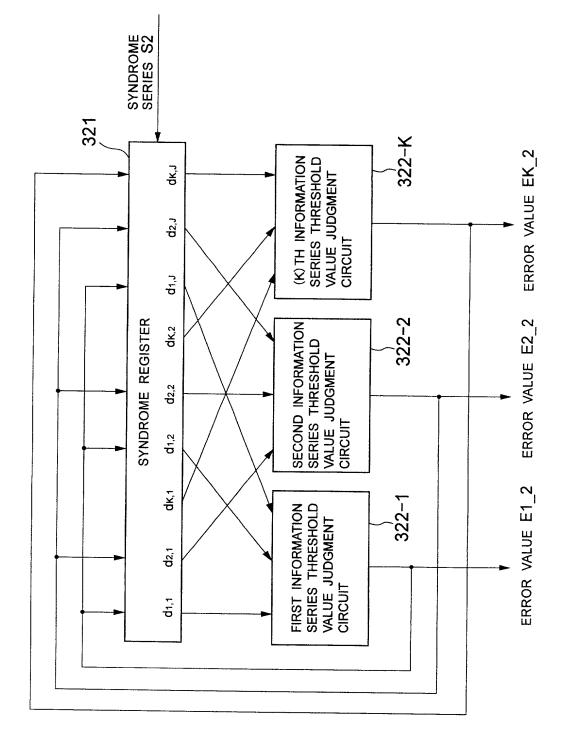
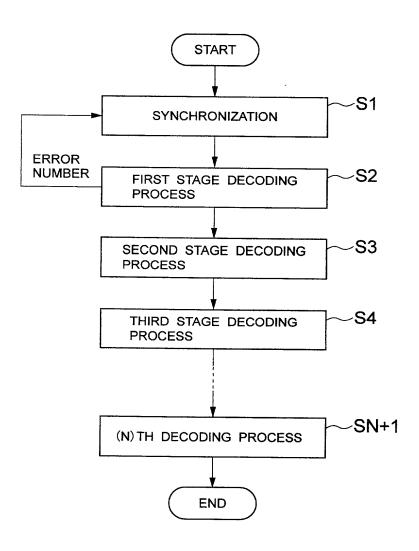
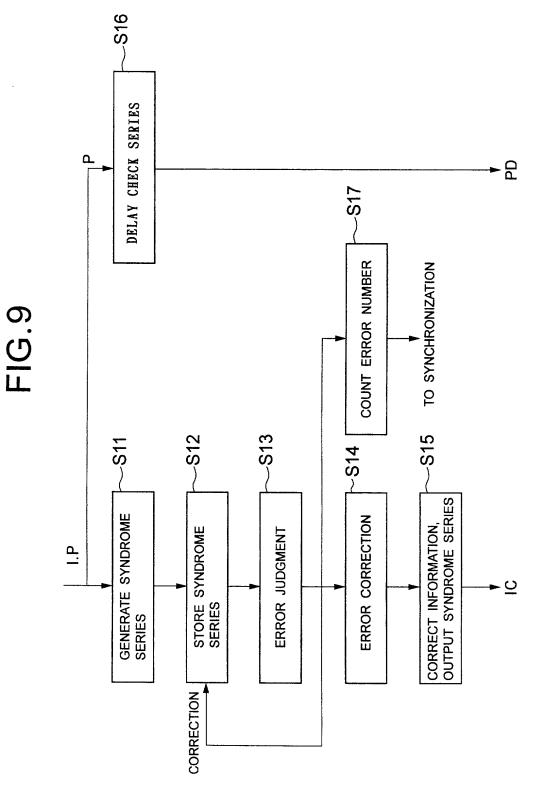


FIG.8





DECODING SERIES FIRST STAGE CORRECTED INFORMATION SECOND STAGE STAGE DECODING CIRCUIT SELF ORTHOGONAL DECODING CIRCUIT STAGE DECODING CIRCUIT FIG. 10 **FIRST** INFORMATION SOURCE CODE SYNCHRONIZATION SERIES I
AND SERIAL / PARALLEL
CONVERTER CIRCUIT CHECK SERIES 73 ENCODER RECEPTION SERIES COMMUNICATION PATH

FIG.11

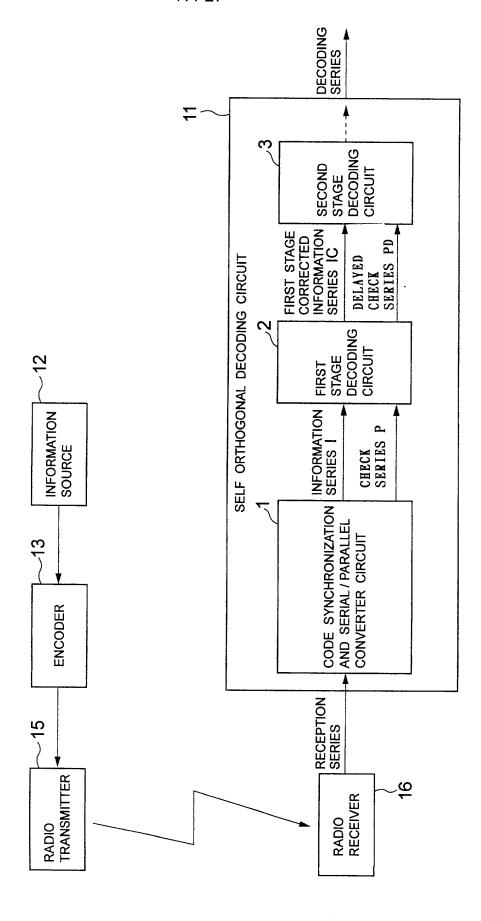
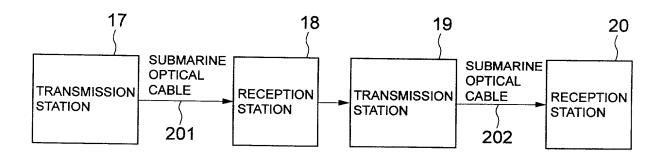


FIG.12



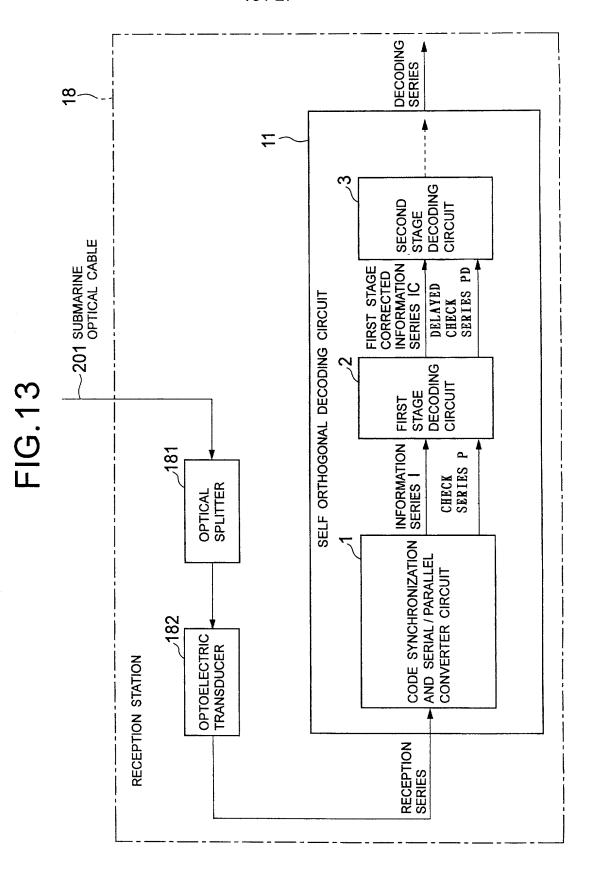


FIG 14

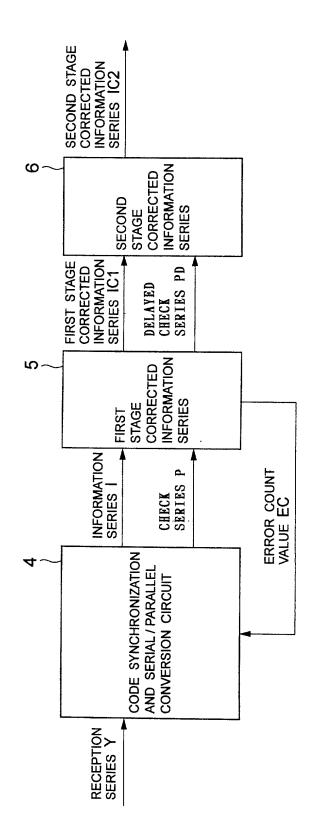


FIG.15

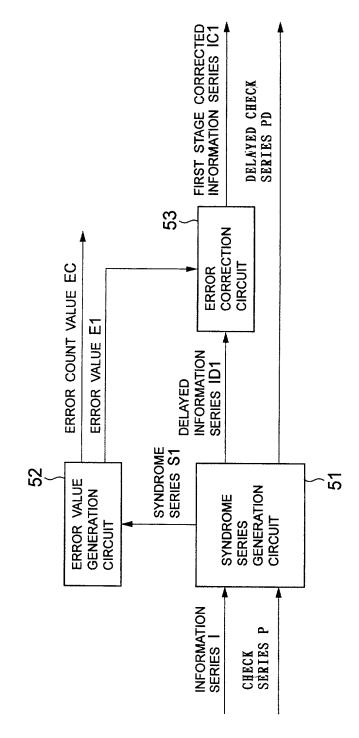


FIG. 16

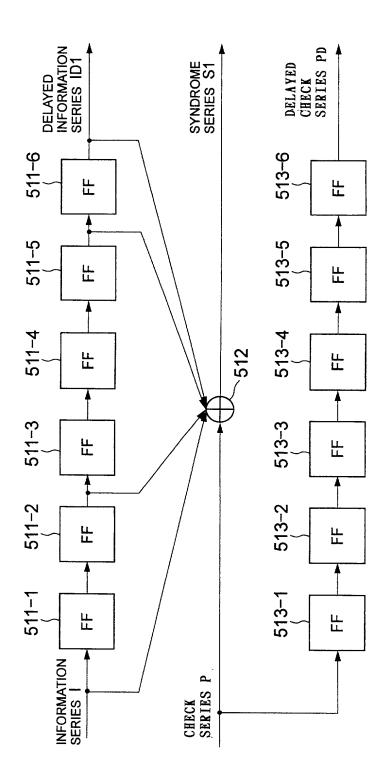
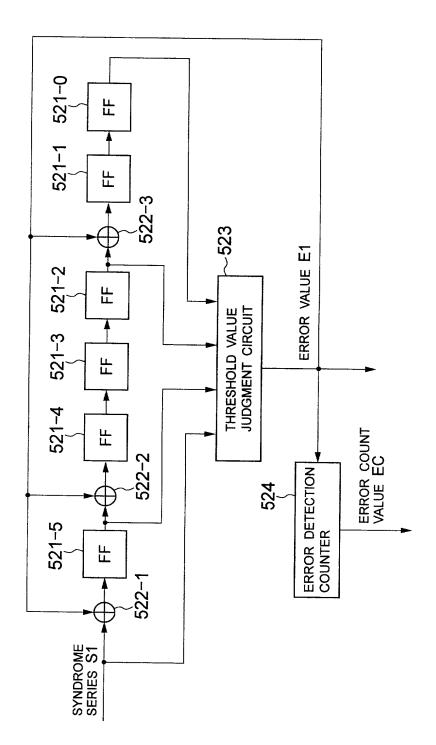


FIG.17



Ź,

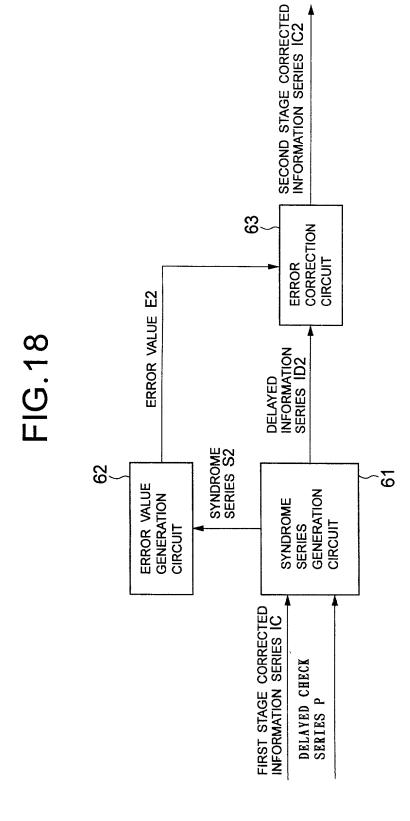


FIG.19

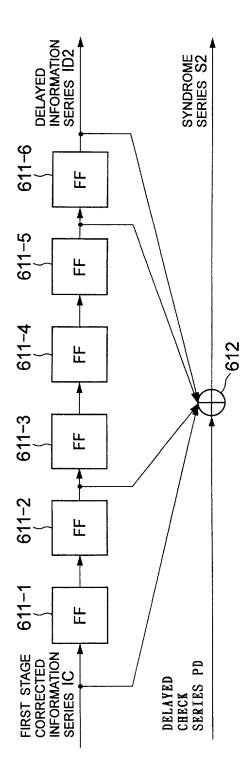


FIG. 20

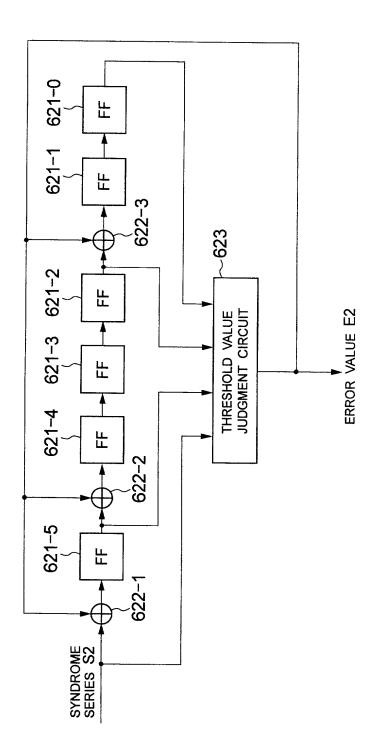
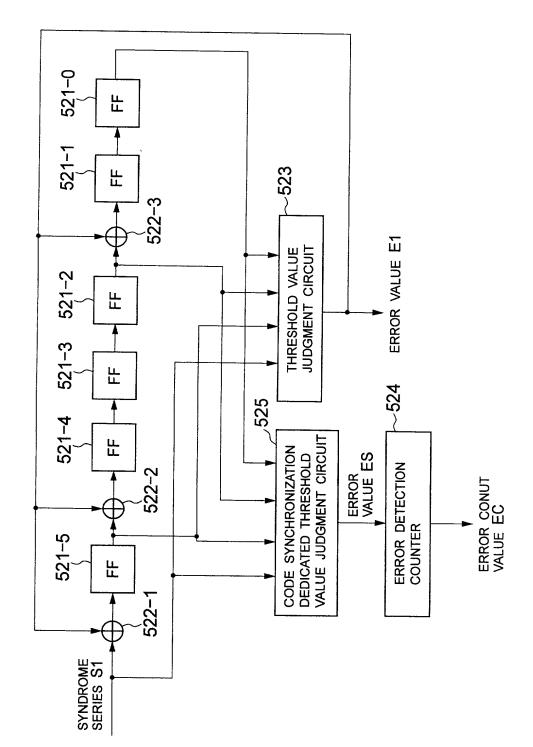
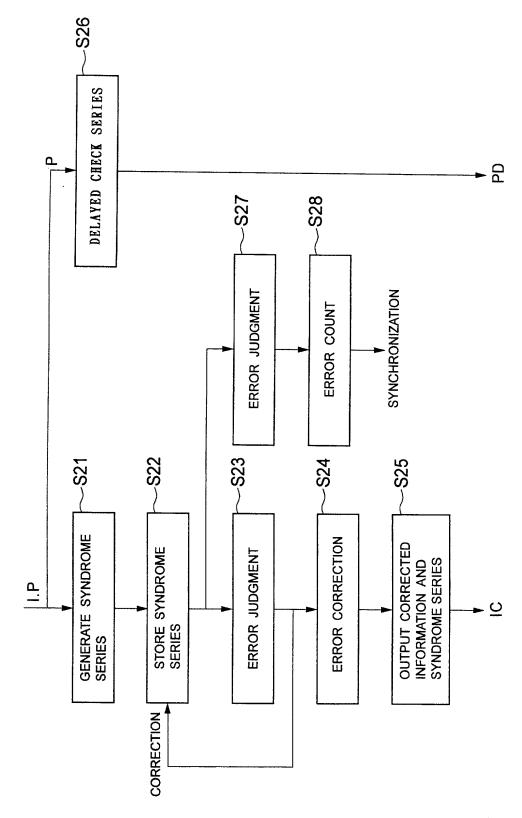
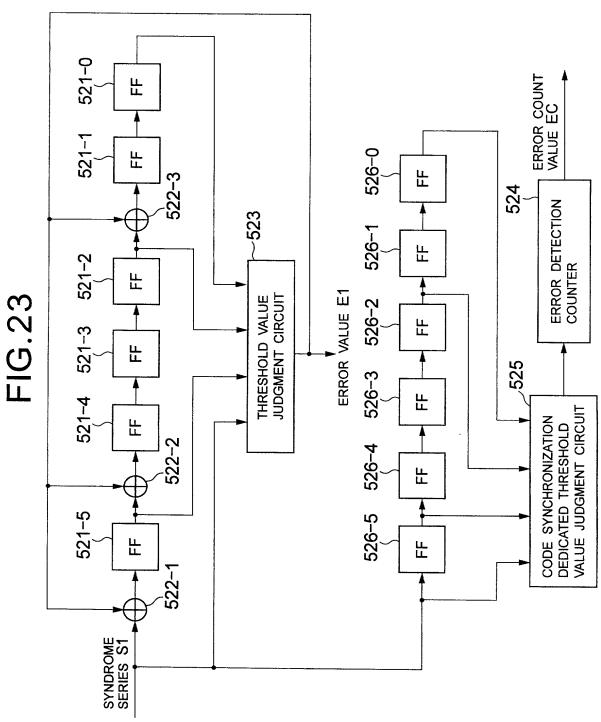


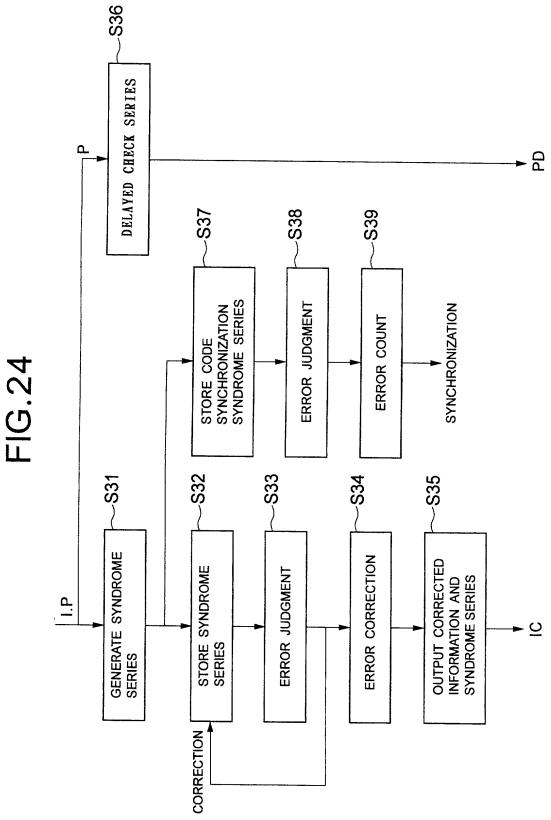
FIG.21











24 / 27

CORRECTED INFORMATION SERIES IC ERROR CORRECTING တ PORTION REGISTER ERROR VALUE E DELAYED INFORMATION SERIES ID SYNDROME SERIES S 10 ERROR VALUE GENERATION CIRCUIT SYNDROME SERIES GENERATION CIRCUIT ∞ INFORMATION SERIES 1 CHECK SERIES P ERROR COUNT VALUE EC CODE SYNCHRONIZATION AND SERIAL / PARALLEL CONVERSION RECEPTION SERIES Y

FIG.26

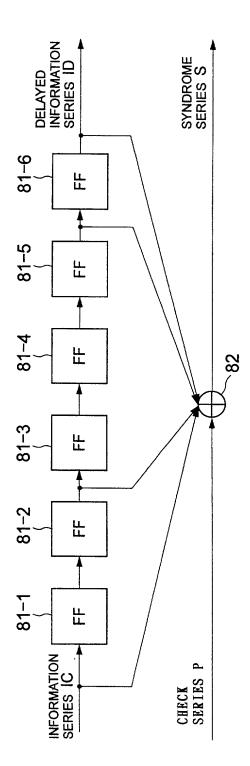


FIG.27

